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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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GRAYBEAL, JACKSON, HALEY LLP
155 - 108TH AVENUE NE
SUITE 350
BELLEVUE, WA 98004-5901

EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,126	BALDI ET AL.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *24-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group II in the reply filed on 03-07-05 is acknowledged. The traversal is on the ground(s) that there is no significant burden on the examiner and certainly no serious burden required by MPEP section 803. This is not found persuasive.

A restriction requirement between one set of product claims and a set of process claims was issued in the Office Action mailed on 17 February 2005. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions', which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See Applied Materials Inc. v. Advanced Semiconductor Materials 40 USPQ2d 1481, 1492 (Fed. Cir. 1996) (Archer, C.J., concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related invention." See In re Taylor, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See In re Berg, 46 USPQ2d 1226, 1233 n. 10 (Fed. Cir. 1998).

1. The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." Applied Materials Inc. at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different

process (MPEP § 806.05(f))." In this application, the examiner restricted the product claims from the process claims on the grounds that "the product as claimed can be made by another and materially different process, such as selectively depositing protective layer to expose a substrate and then forming a second regions in the exposed substrate.and that, as a result, a restriction was necessary.

In addition to one way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." Applied Materials Inc. at 1492. "A serious burden on the examiner may be prima facie shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement is proper because the product claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Applicant has set out no other specific reason, therefore restriction requirement is maintained. Accordingly, the requirement is still deemed proper and is therefore made FINAL.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field June 07, 2004.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13, 15, & 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "said third" in line 2.

Claim 15 recites the limitation "said first implanted region" in line 2.

There are insufficient antecedent basis for this limitation in the claim.

Re claim 17, the phrase "etching said **first spacers** to expose said semiconductor substrate" is misdescriptive. It should be - - etching said first regions- -.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-5, 7, 9-11 & 16-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Gardner et al. (US 6,200,865).

Re claims 1-3 & 17, Gardner et al. teach a method for forming structures self-aligned with each other on a semiconductor substrate, comprising the following steps (Figs.1-9):

Forming, on the semiconductor substrate (10), first regions (12) of a first material projecting from said semiconductor substrate; forming first spacers (22) of a second selectively material with respect to the first material on the sidewalls of said first regions, before protective layer is formed; forming, over the whole of said semiconductor substrate, said protective layer (30, Fig.5) of a third material selective with respect to the second material; removing said protective layer to expose said first regions through a planarizing step (Fig.6); and etching said first regions to expose said semiconductor substrate, and forming second regions projecting from the substrate of said protective layer.

Re claims 4-5, Gardner et al. teach carrying out an implanting step on the whole semiconductor substrate to form, on said semiconductor substrate, first implanted regions (lfg.3) adjacent to said first regions, before the protective layer is formed.

Re claim 5, Gardner et al. teach said first spacers are made of a third material selective with respect to the first material.

Re claim 9, Gardner et al. teach in that planarizing step is carried out by using a CMP technique.

Re claim 10, Gardner et al. teach said first material is a silicon oxide and said second material is silicon nitride (Col.2, lines 50-65).

Re claim 11, Gardner et al. teach said first material is a silicon nitride and said second material is silicon oxide (Col.2, lines 50-65).

Re claim 16, Gardner et al. teach forming, on said semiconductor substrate, a metal layer after said first spacers are formed, and subsequent thermal treatment to

selectively form a silicide layer (28, Fig.4) on the substrate portions, that are exposed from said first regions, and said first spacers. See also Col.6, line 64 – Col.7, line 9.

Re claim 18, Gardner et al. teach a method of forming self-aligned structure in a semiconductor substrate, the method comprising (Figs.1-9):

Forming first regions (12) of a first material on a surface of the semiconductor substrate; forming second regions in exposed portions of the semiconductor substrate, the exposed portions being defined by the first regions of the first material; forming on the first regions and on the exposed portions of the semiconductor substrate third regions of a second material (30, Fig.5), the second material being selectively removable relative to the first material; removing portions of the second material to expose the first regions (Fig.6); removing the first regions to expose corresponding portions of the semiconductor substrate (Fig.7); and forming fourth regions in the exposed portions of the semiconductor substrate.

Re claim 19, Gardener et al. teach the method further comprises forming spacers (22) on sidewalls of the first regions, the spacers being formed from a third material and having a thickness to define a desired distance between each fourth region and adjacent second regions.

Re claim 20, Gardner et al. teach the method further comprising prior to forming the further regions, forming spacers on sidewalls of the third regions, the spacers having a thickness to define a width of the fourth regions subsequently formed.

Re claim 21, Gardner et al. teach the first, second and third regions have dimensions limited by an associated photo lithographic process, and wherein the

thickness of the spacers define widths of the fourth regions that are less than a minimum dimension of the photo lithographic process.

Re claim 22, Gardner et al. teach the first material comprises silicon dioxide and wherein the second material comprises silicon nitride.

Re claim 23, Gardner et al. teach removing portions of the second material comprises planarizing the second material to expose the first regions.

8. Claims 1, 6, 8, 12 & 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeh et al. (US 6,319,807).

Re claim 1, Yeh et al. teach a method for forming structures self-aligned with each other on a semiconductor substrate, comprising the following steps (Fig.2):

forming, on the semiconductor substrate (210), first regions (240A) of a first material projecting from said semiconductor substrate; forming, over the whole of said semiconductor substrate, a protective layer (290, Fig.2H) of a third material selective with respect to the second material; removing said protective layer to expose said first regions through a planarizing step; and etching said first regions to expose said semiconductor substrate, and forming second regions projecting from the substrate of said protective layer (Fig.2I).

Re claim 2, Yeh et al. teach forming first spacers (270) of a second selective material with respect to the first material on the sidewalls of said first regions, before said protective layer is formed.

Re claim 6, Yeh et al. teach forming second spacers (310, Fig.2J) on the sidewalls of said first spacers.

Re claim 8, Yeh et al. teach in that second spacers are made of a fourth material selective with respect to the first material.

Re claim 12, Yeh et al. teach forming an additional protective layer (230, Fig.2A) on the whole said substrate before forming said first regions of a fifth material with respect to the first material.

Re claim 14, Yeh et al. teach said fifth material is silicon oxide.

9. Claims 1 & 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Marty (US 2001/0039095).

Re claim 1, Marty teaches a method for forming structures self-aligned with each other on a semiconductor substrate, comprising the following steps (Fig.1):

forming, on the semiconductor substrate (10), first regions (20) of a first material projecting from said semiconductor substrate; forming, over the whole of said semiconductor substrate, a protective layer (24, Fig.1e) of a third material selective with respect to the second material; removing said protective layer to expose said first regions through a planarizing step; and etching said first regions to expose said semiconductor substrate, and forming second regions projecting from the substrate of said protective layer (Fig.1f).

Re claim 15, Marty teaches a first implanted regions are extrinsic base regions (22) of a bipolar transistor, and that said at least second regions are bipolar transistor emitter and base junctions, respectively.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D.
Primary Examiner
Art Unit 2811

dhk